[NAME OF DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] SEMICONDUCTOR DEVICE WITH Kr-CONTAINING SILICON OXIDE FILM INTEGRATED THEREINTO, AND MANUFACTURING METHOD OF THE SILICON OXIDE FILM

[WHAT IS CLAIMED IS:]

[CLAIM 1]

A semiconductor device including a plurality of transistors having a source region and a drain region of high concentration of impurity region, characterized in that

at least part between the source region and the drain region is made of a silicon oxide film containing Kr.

[CLAIM 2]

The semiconductor device according to claim 1, characterized in that the Kr content in said silicon oxide film is 5×10^{9} cm^{-2} or more and less than 5×10^{11} cm^{-2} at the surface density.

[CLAIM 3]

The semiconductor device according to claim 1 or 2, characterized in that the content of Kr contained in said silicon oxide film decreases from said silicon oxide film surface toward a silicon/silicon oxide film interface.

[CLAIM 4]

A method for forming a silicon oxide film, characterized by introducing a mixture gas mainly containing a gas containing oxygen and Kr gas into a process chamber, exciting plasma with a microwave,

and directly oxidizing a silicon substrate surface placed in the process chamber, thereby forming the silicon oxide film containing Kr in any one of claims 1 to 3 on said silicon substrate surface.

[CLAIM 5]

The method for forming a silicon oxide film according to any one of claims 1 to 4, characterized in that the oxygen partial pressure in said mixture gas is 2 to 4%, and the pressure in said process chamber is 800 mTorr to 1.2 Torr.

[CLAIM 6]

The method for forming a silicon oxide film according to claim 5, characterized in that the plasma recited in claim 4 is plasma excited with a microwave of a frequency of 900 MHz to 10 GHz.

[CLAIM 7]

The method for forming a silicon oxide film according to any one of claims 4 to 6, characterized in that said plasma is plasma excited with using a radial line slot antenna.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[FIELD OF THE INDUSTRIAL AVAILABILITY]

The present invention relates to methods for forming very thin silicon oxide films and semiconductor devices using silicon oxide films.

[0002]

[CONVENTIONAL ART]

[0003]

[PROBLEMS WHICH THE INVENTION IS TO SETTLE]

It is an object of the present invention to form a uniform silicon oxide firm of a high quality on the surface of a substrate at a low substrate-temperature of 200-500°C and to provide semiconductor device using a silicon oxide film.

[0004]

[MEANS FOR SOLVING THE PROBLEMS]

The semiconductor devices (single-crystal, polysilicon, or amorphous semiconductor) formed on a SOI (Silicon on Insulator) substrate including a metal layer or a glass substrate requires a high quality silicon oxide film formed at a low temperature, such as 500-600 °C or less. In recent years, techniques for forming silicon oxide films at low temperatures have been studied. However, since a silicon oxide film formed at low temperature has a high inter level density and low withstand voltage, it cannot be used as a protective film in directly contact with a gate insulating film or semiconductor region of a transistor. The present invention provides a method of forming silicon oxide films having, even though they were formed by low-temperature plasma oxidation, characteristics superior to those of silicon thermal oxide films formed at a high temperature of about 1000°C, and the present invention provide a semiconductor device using the silicon oxide film as a protective film in

directly contact with a gate insulating film and a single-crystal, polycrystal or amorphous semiconductor layers of a transistor.

[0005]

An embodiment of the present invention will be described below.

[EMBODIMENT 1]

[0006]

Low-temperature oxide film formation using plasma will be described first. Fig. 1 is a sectional view showing an example of apparatus using a radial line slot antenna for realizing an oxidation method of the present invention (refer to Japanese Patent Application No. 9-133422). This apparatus is mainly effective for a circular substrate. A vacuum vessel (process chamber) 101 is made vacuous, Kr gas and O_2 gas are introduced through a shower plate 102, and, for example, the pressure in the process chamber is set at about 1 Torr. A circular substrate 103 such as a silicon wafer is placed on a sample table 104 with a heating system, and, for example, setting is made such that the temperature of the sample becomes 200 to 500°C. A microwave of 2.45 GHz is supplied from a coaxial waveguide tube 105 through a radial line slot antenna 106 and a dielectric plate 107 into the process chamber, and high density plasma is generated in the process chamber. The distance between the shower plate 102 and the substrate 103 is set at 6 cm in this embodiment. Although an example

wherein film formation was done using the plasma apparatus with the radial line slot antenna was shown in this embodiment, the microwave may be introduced into the process chamber using another method.

[0007]

In the high density plasma of the mixture gas of Kr and O_2, Kr* in an intermediate excitation state collides with an O_2 molecule, and atomic oxygen O* is efficiently generated. With this atomic oxygen, the substrate surface is oxidized. Until now, for example, oxidation of silicon surfaces was made with H_2O molecules or O_2 molecules, and the process temperatures were very high as 800 to 1100°C. However, oxidation with atomic oxygen is possible at a sufficiently low temperature. To increase opportunities of collision between Kr* and O_2, the higher process chamber pressure is desirable. But, if the pressure is too high, generated O* radicals collide with each other and return to an O_2 molecule. Of course, there is the optimum gas pressure. Fig. 1 shows the oxide film thickness that grows through an oxidation process at a silicon substrate temperature of 400°C for ten minutes, when the gas pressure in the process chamber is changed while the pressure ratio in the process chamber is kept at 97% Kr/3% oxygen. When the gas pressure in the process chamber is 1 Torr, the oxide film becomes the thickest.

[0008]

Fig. 3 shows the relation between the oxide film

thickness and the oxidation time upon silicon substrate surface oxidation using Kr/O_2 high density plasma. Fig. 3 also shows the dependence on the oxidation time in conventional dry oxidation, in relation to substrate temperatures 800°C, 900°C, and 1000°C. It is clear that the oxidation speed of the Kr/O_2 high density plasma oxidation when the substrate temperature is 400°C and the pressure in the process chamber is 1 Torr is higher than that of the atmospheric pressure dry O_2 oxidation when the substrate temperature is 1000°C. Introduction of silicon substrate surface oxidation using Kr/O_2 high density plasma considerably improves productivity of the surface oxidation technique. Further, in a conventional high-temperature thermal oxidation technique, O_2 molecules or H_2O molecules pass through the oxide film formed on the surface, by diffusion. They reach the interface between silicon/silicon oxide film and contribute to oxidation. Thus it was common knowledge that the oxidation speed is greatly influenced by the diffusion speed of O_2 or H_2O molecules in the oxide film, and increases in proportion to $t^{1/2}$ with the oxidation time t. In this case of Kr/O_2 high density plasma, however, the oxidation speed is linear till 35 nm of the oxide film thickness. This shows that atomic oxygen can freely pass through the silicon oxide film. Namely, it is clear that the diffusion speed is very high.

[0009]

Fig. 4 shows a result of an examination in which the distribution along depth of the Kr density in a silicon oxide film formed through the above-described process was examined with a full-reflection fluorescence X-ray spectrometer. The examination was done under the conditions that the partial pressure of oxygen in Kr was 3%, the pressure in the process chamber was 1 Torr, and the substrate temperature was 400°C. The thinner the oxide film thickness is, the more the Kr density decreases. At the silicon oxide film surface, Kr exists at a density of about 2×10^{11} cm^{-2}. That is, this silicon oxide film is a film in which the Kr concentration in the film of the thickness of 4 nm or more is constant and the Kr concentration decreases toward the interface between silicon/silicon oxide film.

[0010]

Fig. 5 shows kinds of rare gases (Kr, Ar, He) used in silicon oxide film growth, and a result of an examination in which the ratio in composition of oxygen to silicon in silicon oxide films obtained was examined with an X-ray photoelectron spectrometer. Formation of the silicon oxide films was done with the apparatus shown in Fig. 1 at a substrate temperature of 400°C. The partial pressure of oxygen in each rare gas and the pressure in the process chamber were fixed at 3% and 1 Torr, respectively. For comparison, the ratio in composition of oxygen to silicon in a thermal oxide film formed at a substrate

temperature of 900°C in the dry oxidation atmosphere is also shown. In case of using helium gas (He) or argon gas (Ar), the composition ratio of the silicon oxide film shows poorness of oxygen. Contrastingly, the silicon oxide film formed using Kr gas shows the ratio of oxygen to silicon equivalent to that of the thermal oxide film. We suspect this is because the excitation state of Kr very efficiently generates O* in comparison with He or Ar.

[0011]

Fig. 6 shows kinds of rare gases used in silicon oxide film growth, and a result of an examination in which the interface level density in silicon oxide films obtained was examined through low-frequency C-V measurement. Formation of the silicon oxide films was done with the apparatus shown in Fig. 1 at a substrate temperature of 400°C. The partial pressure of oxygen in each rare gas and the pressure in the process chamber were fixed at 3% and 1 Torr, respectively. For comparison, the interface level density in a thermal oxide film formed at a substrate temperature of 900°C in the atmosphere of 100% oxygen is also shown. The interface level density of the oxide film formed using Kr gas is the lowest and it is equivalent to the interface level density of the thermal oxide film formed in the dry oxidation atmosphere at 900°C.

[0012]

Fig. 7 shows the relation between kinds of rare

gases and activating energy for silicon oxide film growth calculated from silicon oxide film growing speed. Formation of silicon oxide films was done with the apparatus shown in Fig. 1 at substrate temperatures within the range of 200 to 400°C. The partial pressure of oxygen in each rare gas and the pressure in the process chamber were fixed at 3% and 1 Torr, respectively. In case of oxidation using helium gas (He) and argon gas (Ar), the activating energies are high as 0.5 eV and 0.8 eV, respectively. In case of using Kr gas, however, the activating energy can be held down to 0.13 eV. That is, if the dependence on temperature is very low and atomic oxygen is efficiently generated, even at a low temperature as 200°C, a sufficiently high oxidation speed is realized.

[0013]

Fig. 8 shows a result of examination of the relations between the oxygen partial pressure in Kr in a silicon oxide film formation atmosphere, the withstand voltage of a silicon oxide film, and the interface level density in a silicon oxide film formed. In this case, the pressure in the process chamber was fixed at 1 Torr. When the oxygen partial pressure in Kr is 3%, the interface level density becomes the minimum and its value equivalent to the interface level density in a thermal oxide film is obtained. Besides, the withstand voltage of the silicon oxide film becomes the maximum also in the

vicinity of 3% of the oxygen partial pressure. From the result of Fig. 5, the oxygen partial pressure upon oxidation using Kr/O_2 mixture gas is suitably 2 to 4%.

[0014]

Fig. 9 shows the relations between pressure upon silicon oxide film formation, and the withstand voltage and the interface level density of a silicon oxide film. In this case, the oxygen partial pressure was 3%. When the pressure upon film formation is near 1 Torr, the withstand voltage of the silicon oxide film becomes the maximum and the interface level density becomes the minimum. From this, when an oxide film is formed using Kr/O_2 mixture gas, the pressure upon film formation is optimally 800 to 1200 mTorr.

[0015]

Fig. 10 shows the current-voltage characteristics of 3.5 nm, 5.0 nm, 7.8 nm, and 10 nm-thick silicon oxide films obtained with microwave (2.45 GHz)-excited high density plasma of Kr/O_2 = 97%/3% at a substrate temperature of 400°C when a positive voltage is applied through electrodes to inject electrons into the silicon oxide films from the substrate side. For reference, the characteristics in case of the same thickness and 1000°C dry oxidation are also shown. In the lower electric field region, the electric currents of the silicon oxide films grown with Kr/O_2 are less than those of the thermal oxide films. In

the higher electric field region, both films show quite the same characteristics.

[0016]

Fig. 11 shows the J/E^2-I/E characteristic, i.e., the F-N characteristic when the current density flowing through a silicon oxide film formed with microwave (2.45 GHz)-excited high density plasma of Kr/O_2 = 97%/3% is J (A/cm^2), and the electric field intensity is E (MV/cm). Although three kinds in thickness of silicon oxide films were used, i.e., 5.0 nm, 7.8 nm, and 10 nm, the same characteristic was obtained almost irrespective of film thickness. It is found that F-N currents between 10^{-13} to 10^{-22}, i.e., over the range of nine figures, flow. The barrier height between silicon/silicon oxide films is 3.2 eV.

[0017]

Fig. 12 shows the breakdown fields of silicon oxide films formed with microwave (2.45 GHz)-excited high density plasma of Kr/O_2 = 97%/3%, and 1000°C dry-oxide films in relation to three kinds of films, i.e., 3.5 nm, 5.0 nm, and 7.8 nm as (a), (b), and (c), respectively. In any thickness obtained were quite the same breakdown field intensities as those of the corresponding thermal oxide film.

[0018]

Fig. 13 shows the amounts of charges QBD (Charge-to-Breakdown) till silicon oxide films are broken down when a stress current of 1 A/cm^2 is applied from the substrate side, in relation to Kr/O_2 high density

plasma oxidation, 800°C wet oxidation, and 900°C dry oxidation. The thickness is 5.0 nm. The silicon oxide film grown with Kr/O_2 high density plasma shows its QBD value higher than those of 800°C wet oxidation and 900°C dry oxidation.

[0019]

As for the above-described various characteristics, even though oxidation was done at a low temperature as 400°C, the oxide films grown with Kr/O_2 high density plasma show the characteristics superior to those of the conventional high-temperature thermal oxide films.

[0020]

Fig. 14 shows the subthreshold characteristics of MOS transistors formed on monocrystalline silicon substrates, which figure shows the characteristics when a gate oxide film formed with the apparatus of Fig. 1 using Kr/O_2 high density plasma at a substrate temperature of 400°C and a conventional gate oxide film formed by about 900°C thermal oxidation are used as the gate insulating films. The subthreshold characteristic (marks ○ in the figure) of the MOS transistor with its gate oxide film formed using the apparatus of Fig. 1 shows substantially the same characteristic as the subthreshold characteristic (marks ● in the figure) of the gate oxide film by thermal oxidation.

[0021]

Fig. 15 shows the relation between the drain

current and the gate voltage of MOSFET. In the figure, marks ○ represent a case wherein a Kr/O_2 plasma oxide film is used as the gate insulating film, and, in the figure, marks ● represent a case wherein a thermal oxide film is used as the gate insulating film. The oxide film thickness is 10 nm. Both show quite the same characteristic.

[0022]

It was proved that sufficiently high quality semiconductor device formation is possible using low-temperature formed gate insulating films.

[0023]

Gate oxidation with Kr/O_2 microwave-excited high density plasma using the apparatus of Fig. 1 is optimal for integrated device fabrication on a metallic substrate SOI wafer in which a conventional high-temperature process can not be used.

Fig. 16 is a sectional view of MOS transistors made on a metallic substrate SOI. Reference numeral 1601 denotes n++, p++ low-resistance semiconductor, 1602 does a silicide layer such as NiSi, 1603 does a conductive nitride layer such as TaN or TiN, 1604 does a metal layer such as Cu, 1605 does a conductive nitride layer such as TaN or TiN, 1606 does n++, p++ low-resistance semiconductor layer, 1607 does a nitride insulating film such as AlN or Si_3N_4, 1608 does a SiO_2 film, 1609 does an insulating film of SiO_2, BPSG, or a combination of them, 1610 does an n++ drain region, 1611 does an N++ source region, 1612

does a p++ drain region, 1613 does a P++ source region, 1614 and 1615 do a high-resistance semiconductor layer, 1616 does a SiO_2 film formed with Kr/O_2 microwave-excited high density plasma according to the present invention, 1617 and 1618 do an nMOS gate electrode and a pMOS gate electrode made of, e.g., Ta, Ti, TaN/Ta, TiN/Ti, or the like, 1619 does a nMOS source electrode, and 1620 does nMOS and pMOS drain electrodes. Reference numeral 1621 denotes a pMOS source electrode. Reference numeral 1622 denotes a substrate surface electrode. For the substrate including a Cu layer protected by TaN or TiN, the thermal treatment temperature must be 700°C or less in order to suppress the diffusion of Cu. The n++, p++ source/drain regions are formed by a thermal treatment of 550°C after ion implantation of As+, AsF_2+, or BF_2+. Until now, there was no technique for forming a high-quality oxide film at 700°C or less. By Kr/O_2 microwave-excited high density plasma oxidation, fabrication of the metallic substrate SOIMOSLSI shown in Fig. 16 first became possible.

(Embodiment 2)

[0024]

Fig. 17 is a conceptional view showing an example of apparatus for oxidizing a rectangular substrate such as a glass substrate or a plastic substrate. A vacuum vessel (process chamber) 1707 is put in a depressurized state, Kr/O_2 mixture gas is introduced

through a shower plate 1701, gas is discharged through a thread groove pump 1702, and, for example, the pressure in the process chamber is set at 1 Torr. A glass substrate 1703 is placed on a sample table 1704 with a heating system, and, for example, setting is made such that the temperature of the glass substrate becomes 300°C. A microwave is supplied from a slit of a rectangular waveguide tube 1707 into the process chamber to generate high density plasma in the process chamber. The shower plate 1701 serves also as a waveguide where the microwave radiated from the waveguide tube is propagated to the right and left as a surface wave.

[0025]

Fig. 18 shows a conventional TFT device structure of an inverse-stagger structure and an improved TFT device structure. On the back surface of the glass substrate of the improved TFT device structure, the ITO film 1813 is formed to improve the close contact between the substrate and the susceptor of the film formation apparatus by an electrostatic chuck, and prevent improvement of reliability/uniformity of process, in particular, device break and deterioration of device characteristics due to static electricity. Although a silicon nitride film is used for the gate insulating film 1803 like the prior art, since considerable improvement of its withstand voltage has succeeded, the thickness of the silicon nitride film can be decreased to the degree of 100 to

200 nm though it conventionally required about 400 nm. By thinning the silicon nitride film to a half, it becomes possible to improve the current drive performance of the TFT device substantially twice.

[0026]

In the improved TFT device structure, since not the n+ amorphous silicon layer between the source 1805 and the drain 1807 is etched by RIE, but the n+ amorphous silicon layer is directly oxidized with the apparatus of Fig. 17 to insulate, the non-doped amorphous silicon layer 1804 as the channel is never exposed to high-energy ion irradiation. Therefore, the non-doped amorphous silicon layer 1804 can be thinned from 150 nm to about 30 nm. When the thickness of the non-doped amorphous silicon layer 1804 as the channel becomes 1/5, since the resistance of the spatial charge layer becomes about 1/25, the current drive performance of the TFT device becomes 20 to 30 times. Because the thickness of the non-doped amorphous silicon layer 1804 could be decreased to about 1/5 or less, the amount of generated electron-hole pairs by a back light also could be decreased to about 1/5 or less, and the dynamic range of the luminance of the LCD display section can be improved by nearly one figure.

[0027]

Fig. 19 shows the relation between the gate voltage and the drain current of TFT devices. In comparison with the conventional TFT device, the

drain current of the improved TFT device is considerably increased, and it shows that the characteristic is considerably improved. Simultaneously, the leakage current upon reverse biasing is also decreased. This is because the interface characteristic between the non-doped amorphous silicon and the SiO_2 layer is improved.

[0028]

Fig. 20 shows a sectional structure of polysilicon TFTs made for a peripheral circuit of a display unit such as an LCD. Reference numeral 2001 denotes a glass substrate or a plastic substrate, 2002 does an Si_3N_4 film, 2003 does the channel layer of a polysilicon pMOS, 2005 and 2006 do the source region and the drain region of a polysilicon nMOS, respectively, and 2007 and 2008 do the source region and the drain region of the pMOS, respectively. Reference numeral 2009 denotes a SiO_2 layer according to the present invention, wherein a uniformly thick silicon oxide film at either of its flat portion and its edge portion is formed on polysilicon. Reference numeral 2010 denotes the gate electrode of the polysilicon nMOS, 2011 does the gate electrode of the polysilicon pMOS, 2012 does an insulating film such as SiO_2, BSG, or BPSG, 2013 and 2014 do a source electrode and a drain electrode (simultaneously a drain electrode of the polysilicon pMOS) of the polysilicon nMOS, 2015 does a source electrode of the polysilicon pMOS, and 2016 does a transparent

electrode such as surface ITO.

[0029]

In the apparatus shown in Fig. 17, using a two-stage shower plate microwave-excited high density plasma apparatus in which a two-stage shower plate has been further introduced, when inert gas such as Ar, Kr, or Xe is supplied through the first stage shower plate and material gas such as SiH_4 is supplied through the second stage shower plate, the electron mobility in polysilicon formed is 200 to 400 $cm^2/Vsec$ at a substrate temperature of about 300°C. If the channel length is set at about 1.5 to 2.0 μm, sufficiently high-speed signal processing beyond 100 MHz becomes possible. Most peripheral circuits required for driving a display unit such as an LCD can be made.

[EFFECT]

By using the silicon oxide film formation method of the present invention, a very high-quality silicon oxide film can be formed even though it is formed at a low temperature as a substrate temperature of 200 to 400°C. By this, fabrication of high-performance amorphous silicon TFTs or polysilicon TFTs on a metallic substrate SOILSI, a glass substrate, or a plastic substrate which was conventionally impossible becomes possible, so the effect is great.

[0029]

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1]

Fig. 1 is a conceptional view showing an example of apparatus using a radial line slot antenna for realizing a silicon oxide film formation method of the present invention.

[FIG. 2]

Fig. 2 is a graph showing the dependence of oxidation film thickness on process chamber gas pressure in a high density plasma oxidation process at a substrate temperature of 400°C, Kr/O_2 = 97/3, and 2.45 GHz for ten minutes.

[FIG. 3]

Fig. 3 is a graph showing the dependence of oxidation film thickness on oxidation time in a high density plasma oxidation process at a substrate temperature of 400°C, Kr/O_2 = 97/3, and 2.45 GHz, as well as dependence on oxidation time in conventional dry oxidation (at substrate temperatures of 800°C, 900°C, and 1000°C).

[FIG. 4]

Fig. 4 is a graph showing the distribution along depth of Kr density in a silicon oxide film.

[FIG. 5]

Fig. 5 is a graph showing kinds of rare gases used in silicon oxidation, and ratios in composition of oxygen to silicon in silicon oxide films obtained.

[FIG. 6]

Fig. 6 is a graph showing kinds of rare gases used in growths of silicon oxide films, and a result

of measurement of interface level densities of the silicon oxide films obtained.

[FIG. 7]

Fig. 7 is a graph showing a result of examination of the relation between kinds of rare gases and activating energy for silicon oxide film growth calculated from silicon oxide film growing speed.

[FIG. 8]

Fig. 8 is a graph showing a result of examination of the relations between oxygen partial pressure in Kr in a silicon oxide film formation atmosphere and interface level density in a silicon oxide film formed and its withstand voltage.

[FIG. 9]

Fig. 9 is a graph showing a result of examination of the relations between the whole pressure in a process chamber in a silicon oxide film formation atmosphere and interface level density in a silicon oxide film formed and its withstand voltage.

[FIG. 10]

Fig. 10 is a graph showing the current-voltage characteristics of 3.5 nm, 5.0 nm, 7.8 nm, and 10 nm-thick silicon oxide films obtained with microwave (2.45 GHz)-excited high density plasma of Kr/O_2 = 97%/3% at a substrate temperature of 400°C when electrons have been injected from the substrate side and a positive voltage is applied through electrodes (for reference, the characteristics in case of the same thickness, 1000°C, and dry oxidation are also

shown).

[FIG. 11]

Fig. 11 is a graph showing the J^2/E-I/E characteristic, i.e., the F-N characteristic when the current density flowing through a silicon oxide film formed with microwave (2.45 GHz)-excited high density plasma of Kr/O_2 = 97%/3% is J (A/cm^2), and the electric field intensity is E (MV/cm) (three kinds in thickness of silicon oxide films are used, i.e., 5.0 nm, 7.8 nm, and 10 nm).

[FIG. 12]

In Fig. 12, (a),(b) and (c) are graphs showing the breakdown fields of silicon oxide films formed with microwave (2.45 GHz)-excited high density plasma of Kr/O_2 = 97%/3%, and 1000°C dry-oxide films in relation to three kinds of films, i.e., 3.5 nm, 5.0 nm, and 7.8 nm, respectively.

[FIG. 13]

Fig. 13 is a graph showing the amounts of charges QBD (Charge-to-Breakdown) till silicon oxide films are broken down when a stress current of 1 A/cm^2 is applied from the substrate side, in relation to Kr/O_2 high density plasma oxidation, 800°C wet oxidation, and 900°C dry oxidation.

[FIG. 14]

Fig. 14 is a graph showing the subthreshold characteristics of MOS transistors formed on monocrystalline silicon substrates, which graph shows the characteristics when a gate oxide film formed

with Kr/O_2 high density plasma at a substrate temperature of 400°C and a conventional gate oxide film formed by about 900°C thermal oxidation are used as the gate insulating films.

[FIG. 15]

Fig. 15 is a graph showing the relation between the drain current and the gate voltage of MOSFET (in the figure, marks ○ represent a case wherein a Kr/O2 plasma oxide film is used as the gate insulating film, and, in the figure, marks ● represent a case wherein a thermal oxide film is used as the gate insulating film).

[FIG. 16]

Fig. 16 is a sectional view of MOS transistors made on a metallic substrate SOI.

[FIG. 17]

Fig. 17 is a conceptional view showing an example of apparatus for oxidizing a rectangular substrate such as a glass substrate or a plastic substrate.

[FIG. 18]

Figs. 18 are sectional views showing a conventional TFT device structure and an improved TFT device structure.

[FIG. 19]

Fig. 19 is a graph showing a result of measurement of the relation between the gate voltage and the drain current of TFT devices.

[FIG. 20]

Fig. 20 is a sectional view of polysilicon TFTs

for driving a display section such as an LCD.

[EXPLANETION OF CODES]

101 process chamber

102 shower plate

103 silicon wafer

104 sample table with a heating system

105 coaxial waveguide tube

106 radial line slot antenna

107 dielectric plate

1601 n++, p++ low-resistance semiconductor

1602 silicide layer such as NiSi

1603 conductive nitride layer such as TaN or TiN

1604 metal layer such as Cu

1605 conductive nitride layer such as TaN or TiN

1606 n++, p++ low-resistance semiconductor layer

1607 nitride insulating film such as AlN or Si_3N_4

1608 SiO_2 film

1609 insulating film of SiO_2, BPSG, or a combination of them

1610 n++ drain region

1611 n++ source region

1612 p++ drain region

1613 P++ source region

1614 high-resistance semiconductor layer

1615 high-resistance semiconductor layer

1616 SiO_2 film formed with Kr/O_2 microwave-excited high density plasma according to the present

invention

1617 nMOS gate electrode and a pMOS gate electrode made of, e.g., Ta, Ti, TaN/Ta, TiN/Ti, or the like

1618 nMOS gate electrode and a pMOS gate electrode made of, e.g., Ta, Ti, TaN/Ta, TiN/Ti, or the like

1619 nMOS source electrode

1620 nMOS and pMOS drain electrodes

1621 pMOS source electrode

1622 substrate surface electrode

1701 shower plate

1702 thread groove pump

1703 glass substrate

1704 sample table with a heating system

1705 rectangular waveguide tube

1706 dielectric plate

1801 glass substrate or plastic substrate

1802 gate electrode (Ti/Al/Ti)

1803 gate insulating film (Si_3N_4)

1804 channel (non-doped amorphous silicon)

1805 source (n+ amorphous silicon)

1806 source electrode (Ti/Al/Ti)

1807 drain (n+ amorphous silicon)

1808 drain electrode (Ti/Al/Ti)

1809 interlayer dielectric film (Si_3N_4)

1810 pixel electrode

1811 silicon oxide film for insulating source/drain

1812 gate electrode (TaN/Cu)

1813 transparent electrode on back surface (ITO)

2001 glass substrate or plastic substrate

2002 Si_3N_4 film

2003 channel layer of a polysilicon nMOS

2004 channel layer of a polysilicon pMOS

2005 source region of a polysilicon nMOS

2006 drain region of a polysilicon nMOS

2007 drain region of a polysilicon pMOS

2008 source region of a polysilicon pMOS

2009 SiO_2 film

2010 gate electrode of a polysilicon nMOS

2011 gate electrode of a polysilicon pMOS

2012 insulating film such as SiO_2, BSG, or BPSG

2013 source electrode of a polysilicon nMOS

2014 drain electrode

2015 source electrode of a polysilicon pMOS

2016 transparent electrode such as surface ITO